IN THE CLAIMS:

Amend claim 4 as shown in the following listing of claims, which replaces all prior versions and listings of claims.

1. (canceled).

2. (previously presented) A method of manufacturing a semiconductor integrated circuit in which a CMOS transistor is formed on a first conductivity type semiconductor film provided on a first conductivity type supporting substrate through an embedded insulating film, comprising the steps of:

conducting thermal oxidation to form a LOCOS for element separation between transistors in the semiconductor film;

forming a gate oxide film of a second conductivity type transistor;

forming a first conductivity type impurity region between the gate oxide film and the embedded insulating film in a region where the second conductivity type transistor is to be formed;

forming a polysilicon film on the gate oxide film and etching the polysilicon film so as to form a gate electrode of the second conductivity type transistor;

forming a second conductivity type impurity region in an ultra-shallow portion of each of a source region and a drain region;

forming a second conductivity type impurity region having a low density in a middle portion of each of the source region and the drain region;

forming a second conductivity type impurity region having the same density as the second conductivity type impurity region in the ultra-shallow portion in a lower portion of each of the source region and the drain region; and

providing resist as a mask on a part of the source region and the drain region adjacent to the gate electrode, and further performing ion implantation so as to form a second conductivity type impurity region in each of the source region and the drain region.

3. (previously presented) A method of manufacturing a semiconductor integrated circuit in which a CMOS transistor is formed on a first conductivity type semiconductor film provided on a first conductivity type supporting substrate through an embedded insulating film, comprising the steps of:

conducting thermal oxidation to form a LOCOS for element separation between transistors in the semiconductor film;

forming a gate oxide film of a second conductivity type transistor;

forming a first conductivity type impurity region between the gate oxide film and the embedded insulating film in a region where the second conductivity type transistor is to be formed;

forming a first conductivity type impurity region having a higher density than that of the first conductivity type impurity region in a middle depth portion of the semiconductor film serving as the proximal region to a drain in the first conductivity type impurity region;

forming a polysilicon film on the gate oxide film and etching the polysilicon film so as to form a gate electrode of the second conductivity type transistor; and

performing ion implantation through the gate electrode so as to form a second conductivity type impurity region in each of a source region and a drain region.

4. (currently amended) A semiconductor integrated circuit in which a CMOS transistor is formed on a first conductivity type semiconductor film provided on a first conductivity type supporting substrate through an embedded insulating film, the semiconductor integrated circuit comprising:

a second conductivity type source region and a second conductivity type drain region formed in the semiconductor film;

a gate insulating film formed on an upper surface of the semiconductor film; and

a gate electrode formed on an upper surface of the gate insulating film;

wherein the source region includes an ultra-shallow high-density N-type source extension region at a boundary with a channel region, a low-density N-type source extension region under the ultra-shallow high-density N-type source extension region, and an embedded insulating neighboring N-type source extension region, the source extension regions being stacked in a thickness direction of the semiconductor film; and

wherein the drain region includes an ultra-shallow high-density N-type drain extension region at a boundary with the channel region, a low-density N-type drain extension region under the ultra-shallow high-density N-type drain extension region, and an embedded insulating neighboring N-type drain extension region, the drain extension regions being stacked in a thickness direction of the semiconductor film.

5. (previously presented) A semiconductor integrated circuit according to claim 4; further comprising a first sidewall disposed around the gate electrode and a second sidewall disposed on the first sidewall.

6. (previously presented) A semiconductor integrated circuit in which a CMOS transistor is formed on a first conductivity type semiconductor film provided on a first conductivity type supporting substrate through an embedded insulating film, the semiconductor integrated circuit comprising:

a second conductivity type source region and a second conductivity type drain region formed in the semiconductor film;

a gate insulating film formed on an upper surface of the semiconductor film; and

a gate electrode formed on an upper surface of the gate insulating film;

wherein a channel region disposed under the gate insulating film has a first conductivity type impurity region having a higher density than a well at a boundary with the drain region.